Duco van Amstel

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Education

Ph.D Computer Science *Université Grenoble Alpes*, Grenoble, France — Expected 07 / 2016

MSc. Computer Science *École Normale Supérieure de Lyon*, Lyon, France — 06 / 2012
Passed with high honours (*mention "bien"*)

Bsc. Computer Science *École Normale Supérieure de Lyon*, Lyon, France — 06 / 2010
Passed with high honours (*mention "bien"*)
The *École Normale Supérieure* (ENS) is the most competitive French research school and university.

Preparatory Classes *Louis le Grand*, Paris, France — 2006 - 2009
Intensive program preparing for the competitive entry exams to French engineering schools.
Louis le Grand frequently ranks 1st among the schools offering such a program.

Employment

2013 – 2016 — **R&D engineer**, *Kalray*, Grenoble, France
Kalray is a fabless semi-conductor company designing and supporting its own manycore processors: the MPPA family. This industry position accounted for half of my time as Ph.D student and allowed the implementation of my research work in an industrial environment.
Responsabilities: compiler engineering (GCC & other tools), design and modelisation of a Network-on-Chip, developement and reporting for large scale collaborative projects.

2013 – 2016 — **Research assistant**, *Inria*, Grenoble, France
Member of the Corse research team as part of my Ph.D. Development of heuristical tiling solvers, LLVM passes and the GraphUtilities library for convex partitioning and reachability queries.
Other assignments: system adminstrator & IT purchases

2013 – 2016 — **Teaching assistant**, *Université Grenoble Alpes / ENSIMAG*, Grenoble, France
Independent from my Ph.D work. Assisting in multiple courses.

2012 March – June — **MSc. intern**, *Laboratoire d'Informatique de Grenoble*, Grenoble, France
Work on the Berkeley Open Infrastructure for Network Computing (BOINC).

2011 March – August — **MSc. intern**, *Kalray*, Grenoble, France
R&D for an architecture-specific bitslice implementation of the AES cryptographic protocol.

2010 June – July — **BSc. intern**, *Inria*, Grenoble, France
Traffic flow modeling and prediction. Extension and simulation of a mathematical flow model.

Research interests

Low-level & target-specific optimizations Tweaking code at instruction level, manually or with compilers, to achieve high performance and efficiency. Exploiting target specifics to reduce code size and execution time.

Micro-architecture Studying interactions between a compiler toolchain and a target architecture. Improving the adequacy of the features offered by an architecture with respect to the needs of a compiler.

Graph algorithmics Computation of graph characteristics, analysis of graph structures and other graph-based queries: reachability on DAGs, convex partitioning.

Heuristical approaches Designing low complexity algorithms to compute potentially sub-optimal but efficient solutions to hard problems.

Publications

Conferences & workshops

[1] Łukasz Domagała, Duco van Amstel, and Fabrice Rastello. "Generalized cache tiling for dataflow programs". In: *Proceedings of the 17th ACM SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems*. LCTES '16. (Acceptance rate 27% – 12/44). Santa Barbara, CA, USA: ACM, 2016.

[2] Łukasz Domagała, Duco van Amstel, Fabrice Rastello, and P. Sadayappan. "Register allocation and promotion through combined instruction scheduling and loop unrolling". In: *Proceedings of the 25th Conference on Compiler Construction*. CC '16. (Acceptance rate 31% – 24/77). Barcelona, Spain: ACM, 2016, pp. 143–151.

[3] Benoît Dupont de Dinechin, Yves Durand, Duco van Amstel, and Alexandre Ghiti. "Guaranteed Services of the NoC of a Manycore Processor". In: *Proceedings of the 2014 International Workshop on Network on Chip Architectures*. NoCArc '14. (Acceptance rate 41% – 9/22). Cambridge, UK: ACM, 2014, pp. 11–16.

[4] Benoît Dupont de Dinechin, Duco van Amstel, Marc Poulhiès, and Guillaume Lager. "Time-Critical Computing on a Single-Chip Massively Parallel Processor". In: *Proceedings of the 17th conference on Design, Automation and Test in Europe*. DATE '14. (Acceptance rate 23% – 206/890). Dresden, Germany: European Design and Automation Association, 2014, 97:1–97:6.

Thesis

[5] Duco van Amstel. "Data Locality on Manycore Architectures". PhD thesis. Université Grenoble Alpes, July 2016 (Submitted).

[6] Duco van Amstel. "Scheduling for Volunteer Computing on the BOINC Server Infrastructure". MA thesis. Ecole Normale Supérieure de Lyon, June 2012.

Patents

[7] Duco van Amstel, Alexandre Blampey, and Benoît Dupont de Dinechin. *Token Bucket Flow-Rate Limiter*. Filed 2015.

Software

GraphUtilities library A library developed during my Ph.D for the manipulation and analysis of directed graphs. Its main features are fast multi-threaded reachability querying and convex partitioning.
Available on GitHub at `https://github.com/Helcaraxan/GraphUtilities`.

LLVM generalized tiling Set of LLVM passes and tiling solvers which implement generalized register tiling as described in [2]. Work done together with co-author Łukasz Domagała. My contribution includes among other features the design and implementation of the heuristical tiling methods presented in [1, 5].
Not publicly available. Used by the CORSE research team @ Inria.

Kalray toolchain I made numerous contributions to the global software toolchain that supports the Kalray MPPA manycore chip. The main focus of these contributions were in the area of the specialized GCC back-end and other external code optimization tools. Also includes a simulator for the MPPA Network-on-Chip.
Not publicly available. Part of Kalray's software products.

References

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Fabrice Rastello – Research team leader @ *Inria*, Grenoble, France
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Reviewing

External reviewer DATE'16, CGO'15, CGO'14

Awards & grants

2016	ACM Student Research Competition @ CGO '16 – 2nd place
2013	Selected for a 3-year CIFRE Ph.D funding

Teaching experiences

Introduction to Algorithmics and C Undergraduate - 1st semester Fall 2014
Introductory course for first-year CS students. Core concepts of computer programming and algorithmics.
Responsible for teaching, practice sessions and grading for a single student group (∼40 students)

Logical Circuitry & Processor Architecture Undergraduate - 5th semester Fall 2013 – 2015
Third-year course teaching the basics of circuitry design to software engineering students. The semester finishes with the specification of a small CISC processor and its simulation.
Responsible for practice sessions and part of grading (∼40 students)

Advanced Algorithmics Undergraduate - 6th semester Spring 2013 – 2015
First-year course at the ENSIMAG engineering school (∼3rd year of college). Various data structures and their algorithmic properties.
Responsible for grading of small student projects (∼140 students)

Team-based end-of-year projects Undergraduate - 6th semester Spring 2013 – 2016
First-year course at the ENSIMAG engineering school (∼3rd year of college). Full-time 2-week team coding projects. Various subjects: graphical interface library, MIPS simulator, ...
Member of a 10-person staff advising and grading (∼300 students)

Languages

English - *fluent*, French - *fluent*, Dutch - *mothertongue*, German - *working knowledge*, Swedish - *beginner*