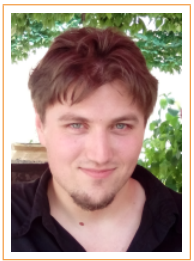
Duco van Amstel

4 A Rue des Routoirs
38610 Gières, France
+33 (0)6 78 31 32 33
duco.van.amstel@ens-lyon.org
www.helcaraxan.eu



Life is an immense Do-It-Yourself box with everything in it...
except for a manual

Experience

Vocational

2013–2016 **R&D engineer**, *Kalray S.A*, Grenoble.

An engineering position combined with a Ph.D research program. Assignments included:

- Compiler R&D (GCC, LLVM & other tools)
  - Design and implementation of compiler optimization passes from scratch
  - Continuing the design and implementation of an in-house optimization tool
  - Fine-tuning of the GCC back-end for the Kalray architecture
- Expertise and design of a Network-on-Chip architecture (including a filed patent)
- Reporting for large-scale collaborative projects

2013–2016 **Teaching Assistant**, *Université Grenoble Alpes*, Grenoble.

T.A for courses at the Université Grenoble - Alpes and the ENSIMAG engineering school.

- Introduction to programming and algorithmics
- Advanced algorithmics
- Logical circuitry and hardware design
- End-of-year programming project

2012 March–June **MSc. Intern**, *LIG*, Grenoble.

Work on the Berkeley Open Infrastructure For Network Computing (BOINC).

- Research & implementation of new scheduling policies for small to medium size projects.

2011 March–August **MSc. Intern**, *Kalray*, Grenoble.

Internship in R&D.

- Architecture-specific bitslice implementation of the AES
- Participated in design of a high-speed Ethernet traffic load-balancer
- Instruction Set Architecture testing on hardware simulator

2010 June–July **BSc. Intern**, *Inria*, Grenoble.

Work on traffic flow modeling and prediction.

- Extension of a mathematical flow model
- Prototype implementation of full scale flow simulator

Miscellaneous

2010–2012 **Event & Technical support coordinator**, *BREI Lyon - Pôle musique*, Lyon.

- Head of technical staff for small and medium scale events
- Organization of technical back-line in collaboration with contractors
- Live sound engineer

2005–2012 **Private tutoring**, *Self-employed*.

- Accompagnying students from high-school to bachelor level in multiple subjects

Education

2013–2016 **Ph.D Computer Science**, *Université Grenoble-Alpes*, Grenoble, Expected July 2016.

Subject: Data Locality on Manycore Architectures

2010–2012 **MSc. Computer Science**, *École Normale Supérieure de Lyon*, Lyon.
Covered topics: Parallel computing, grids, network algorithmics, cryptography, embedded systems, compiler theory, software development, project management

2009–2010 **BSc. Computer Science**, *École Normale Supérieure de Lyon*, Lyon.
The *École Normale Supérieure* is the most competitive French research school and university.
Covered topics: Processor architecture, algorithmics, programming practice, operating systems

2006–2009 **"Classes préparatoires" MPSI-MP***, *Louis le Grand*, Paris.
Intensive program preparing for the competitive entry exams to French engineering schools.
Louis le Grand frequently ranks 1st in France among the schools offering such a program.
Covered topics: Applied mathematics, physics, chemistry, computer science

Computer skills

OS	Linux, Windows	Communication	LaTeX, LibreOffice, Word, PowerPoint, Excel
Programming	C, C++, assembly, Bash	Libraries	pthread, MPI, Qt
Compilers	GCC, LLVM	Other	System & network administration

References

Conferences & workshops

Łukasz Domagała, Duco van Amstel, and Fabrice Rastello. "Generalized cache tiling for dataflow programs". In: *Proceedings of the 17th ACM SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems*. LCTES '16. (Acceptance rate 27% – 12/44). Santa Barbara, CA, USA: ACM, 2016.

Łukasz Domagała, Duco van Amstel, Fabrice Rastello, and P. Sadayappan. "Register allocation and promotion through combined instruction scheduling and loop unrolling". In: *Proceedings of the 25th Conference on Compiler Construction*. CC '16. (Acceptance rate 31% – 24/77). Barcelona, Spain: ACM, 2016, pp. 143–151.

Benoît Dupont de Dinechin, Yves Durand, Duco van Amstel, and Alexandre Ghiti. "Guaranteed Services of the NoC of a Manycore Processor". In: *Proceedings of the 2014 International Workshop on Network on Chip Architectures*. NoCArc '14. (Acceptance rate 41% – 9/22). Cambridge, UK: ACM, 2014, pp. 11–16.

Benoît Dupont de Dinechin, Duco van Amstel, Marc Poulhiès, and Guillaume Lager. "Time-Critical Computing on a Single-Chip Massively Parallel Processor". In: *Proceedings of the 17th conference on Design, Automation and Test in Europe*. DATE '14. (Acceptance rate 23% – 206/890). Dresden, Germany: European Design and Automation Association, 2014, 97:1–97:6.

Thesis

Duco van Amstel. "Data Locality on Manycore Architectures". PhD thesis. Université Grenoble Alpes, July 2016 (Submitted).

Duco van Amstel. "Scheduling for Volunteer Computing on the BOINC Server Infrastructure". MA thesis. Ecole Normale Supérieure de Lyon, June 2012.

Patents

Duco van Amstel, Alexandre Blampey, and Benoît Dupont de Dinechin. *Token Bucket Flow-Rate Limiter*. Filed 2015.

Languages

Dutch	**Native**	*Mother-tongue*
French	**Fluent**	*Oral & written skills*
English	**Fluent**	*Oral & written skills*
German	**Intermediate**	*Good oral & written comprehensive skills*
Swedish	**Beginner**	*Starting level*

Interests

Reading	Novels, science-fiction, fantasy
Sports	Hiking, skiing, paragliding
Technology	Network technology, cryptography, hardware developments